

Fig. 1

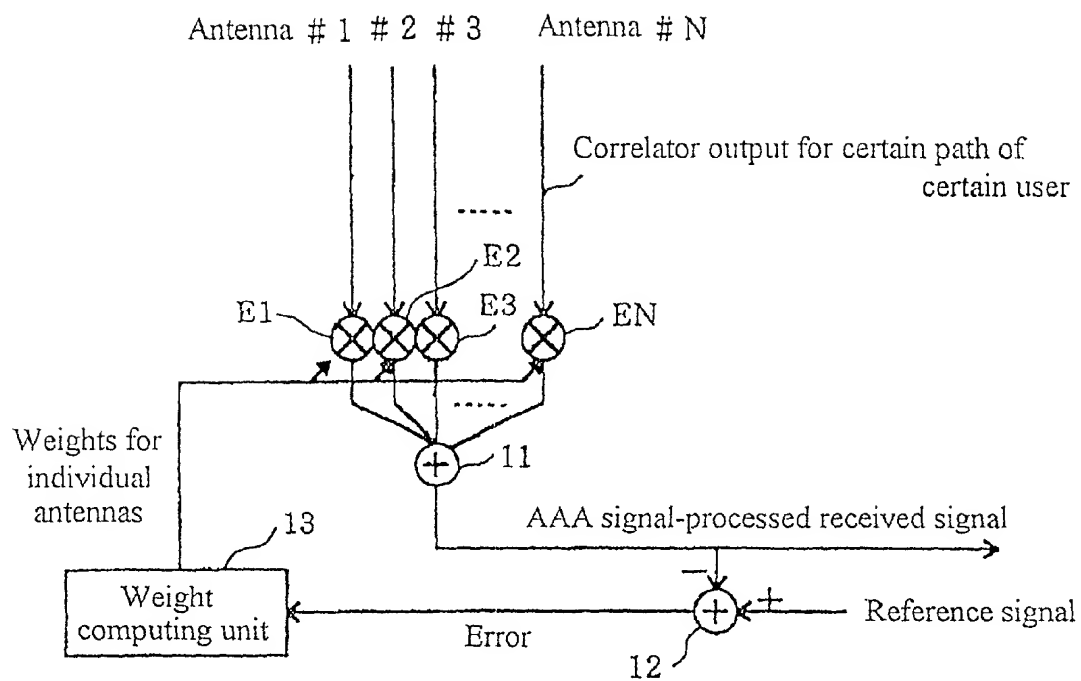


Fig. 2

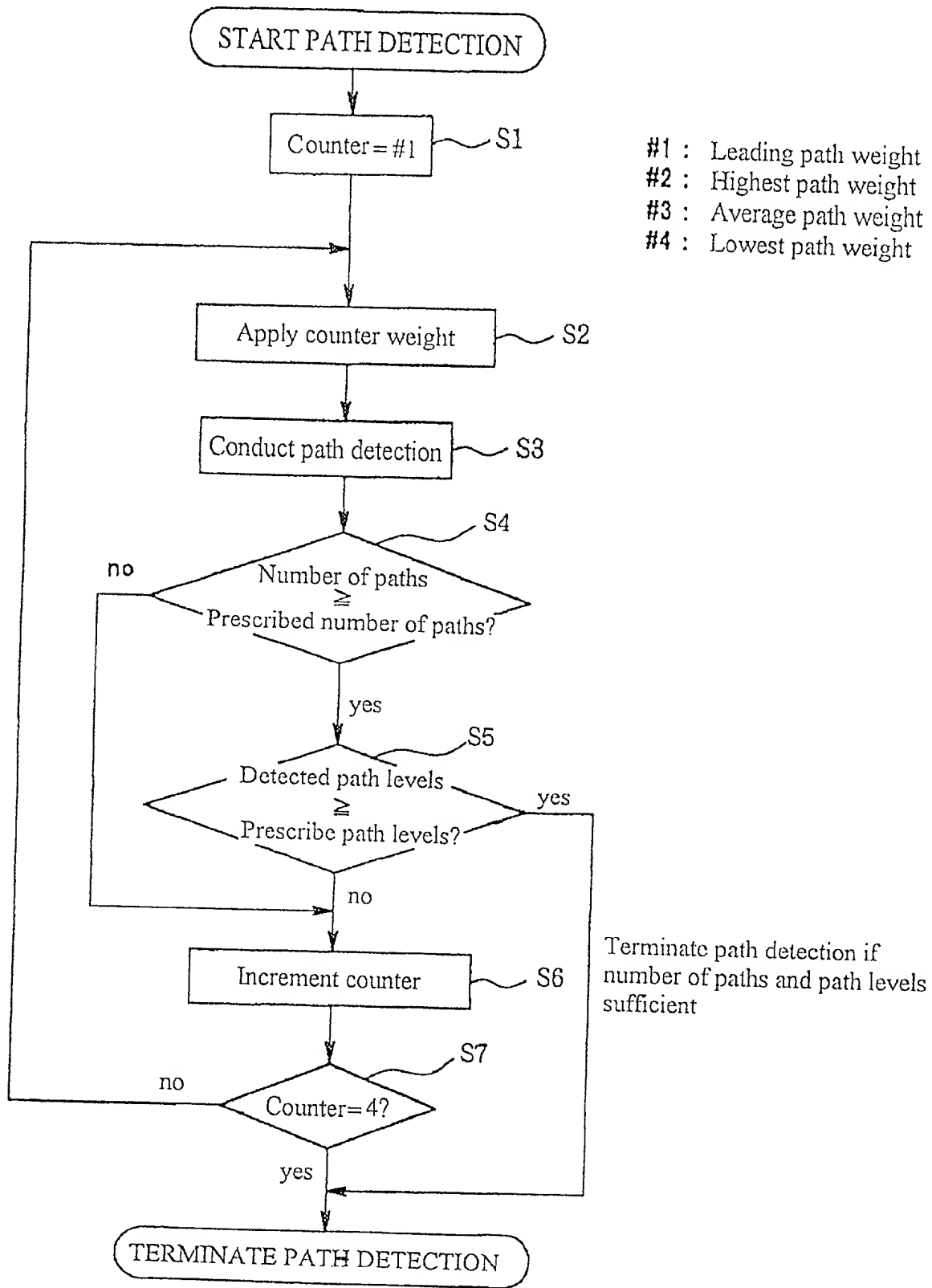
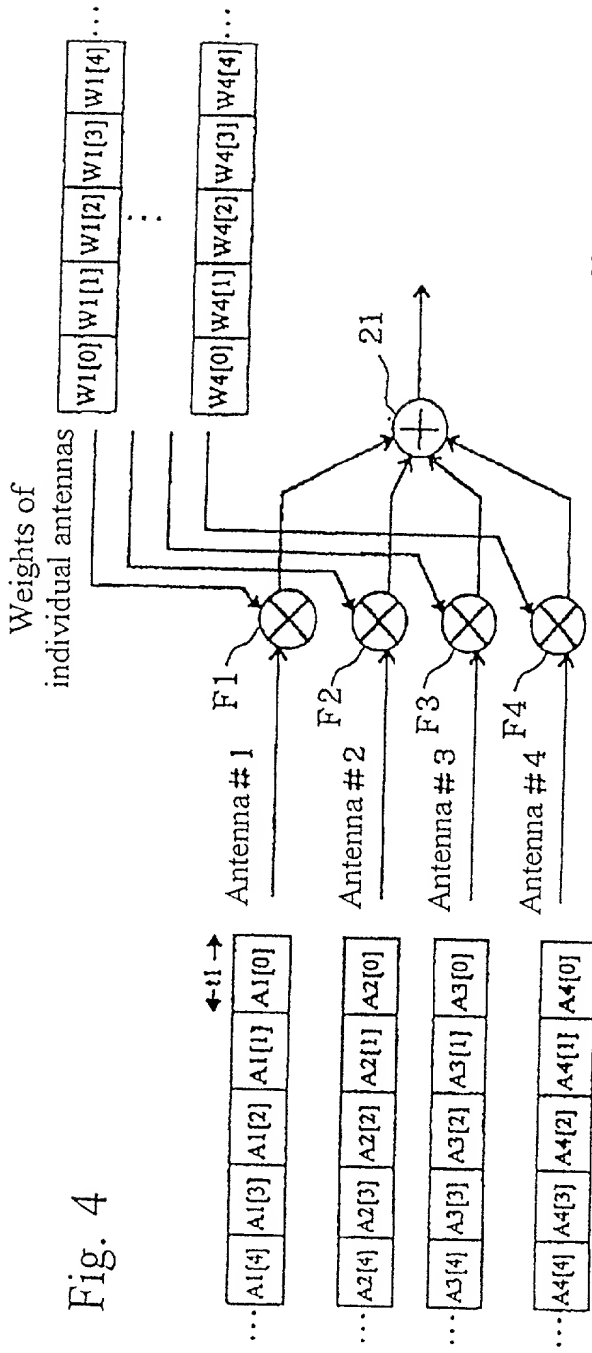


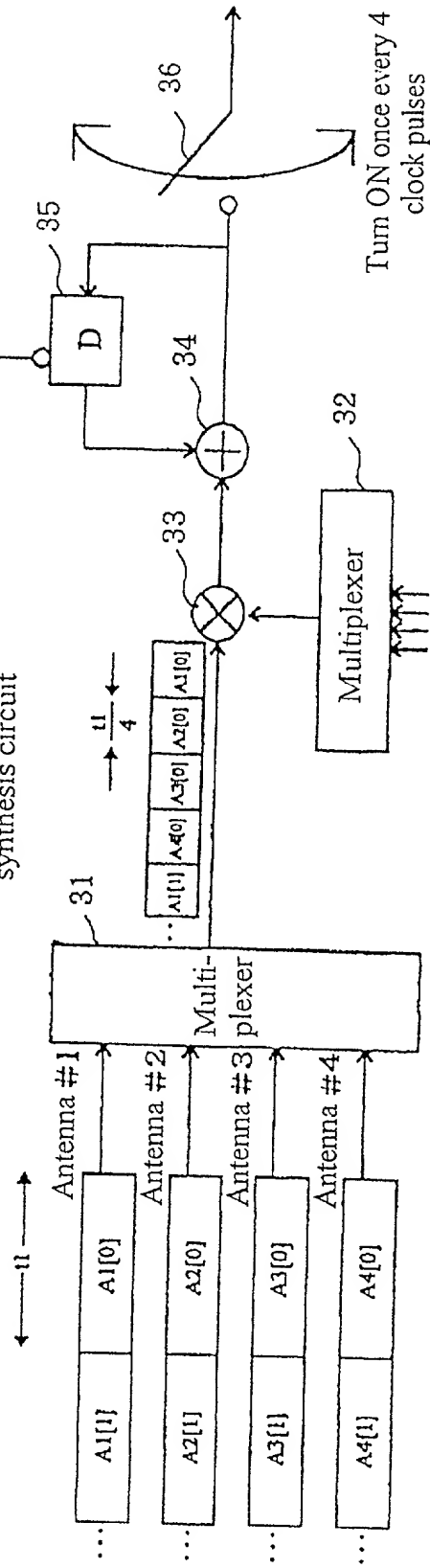
Fig. 3

Fig. 4



Clear to 0 once every 4 clock pulses

(a) Ordinary weight multiplication & synthesis circuit



(b) Weight multiplication & synthesis circuit using time division



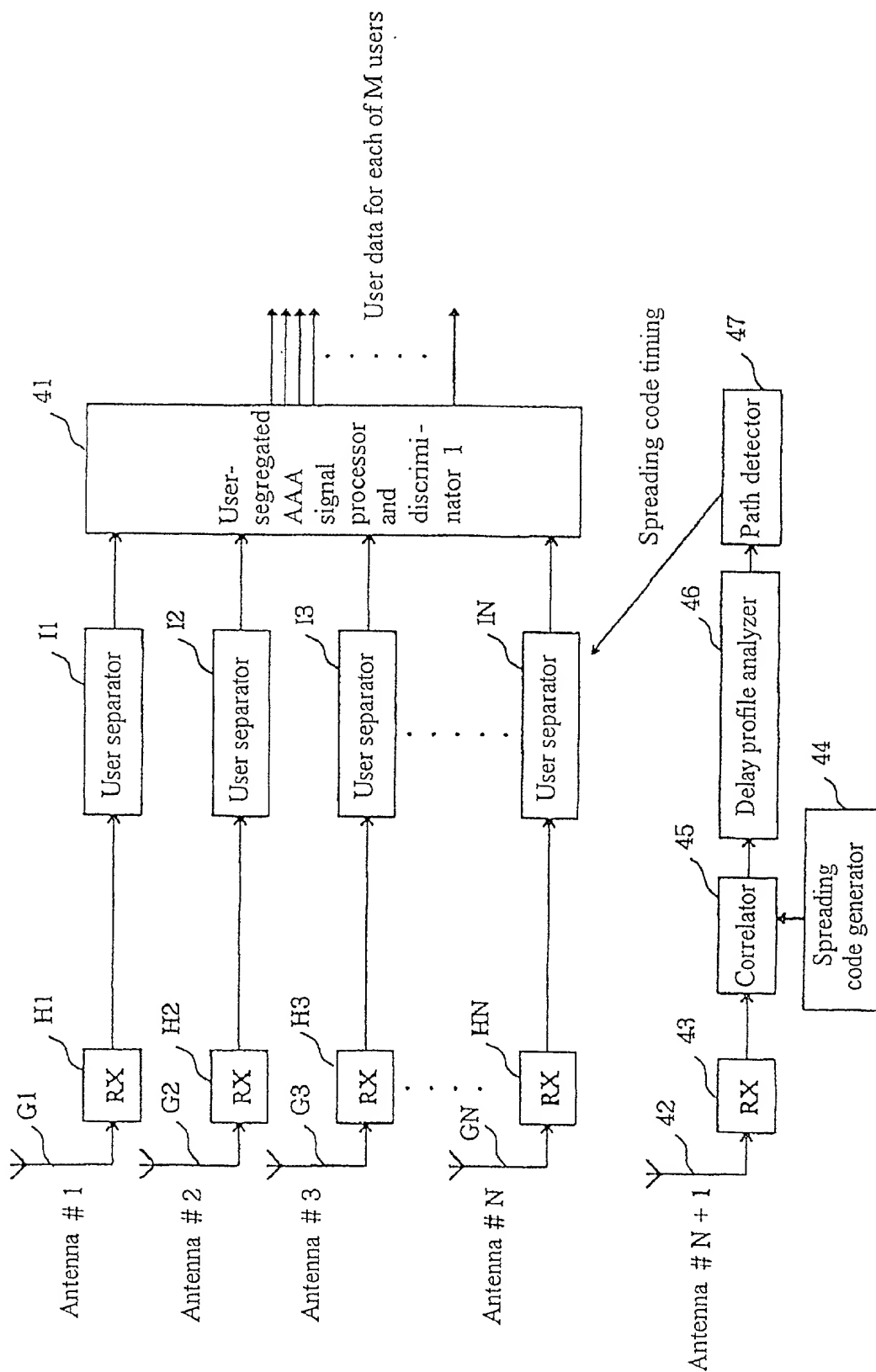


Fig. 6

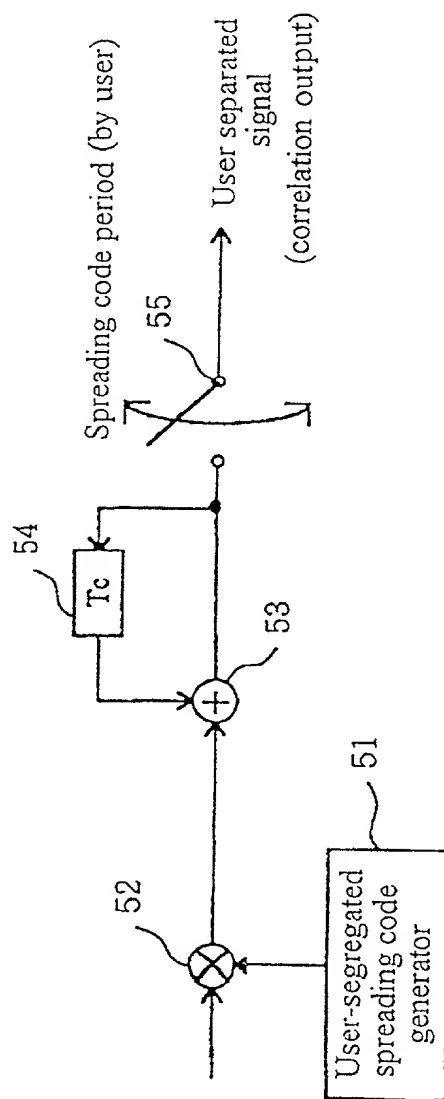


Fig. 7

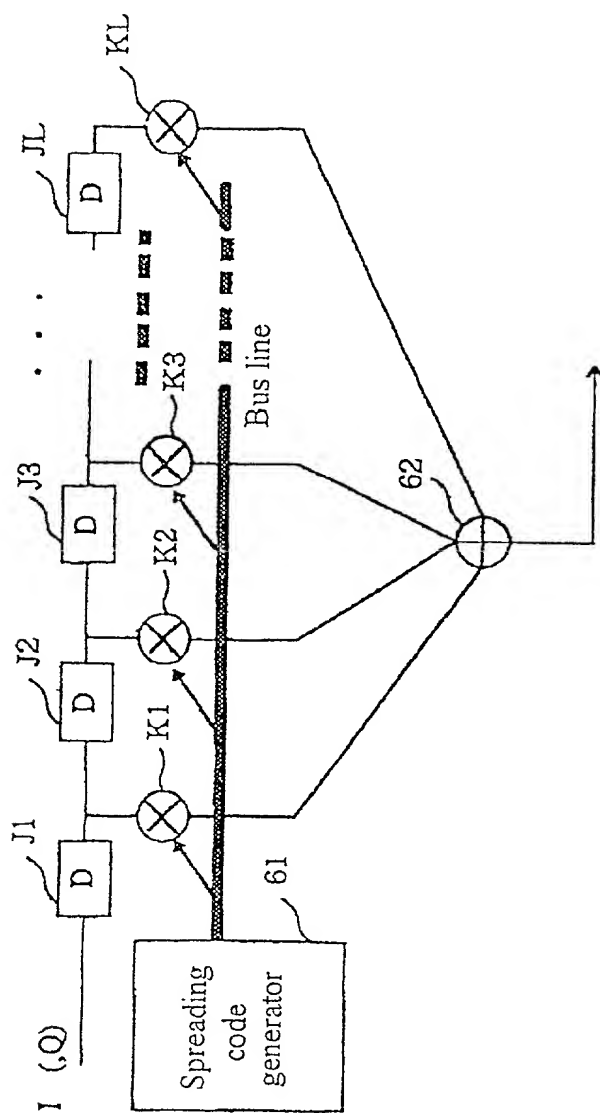


Fig. 8



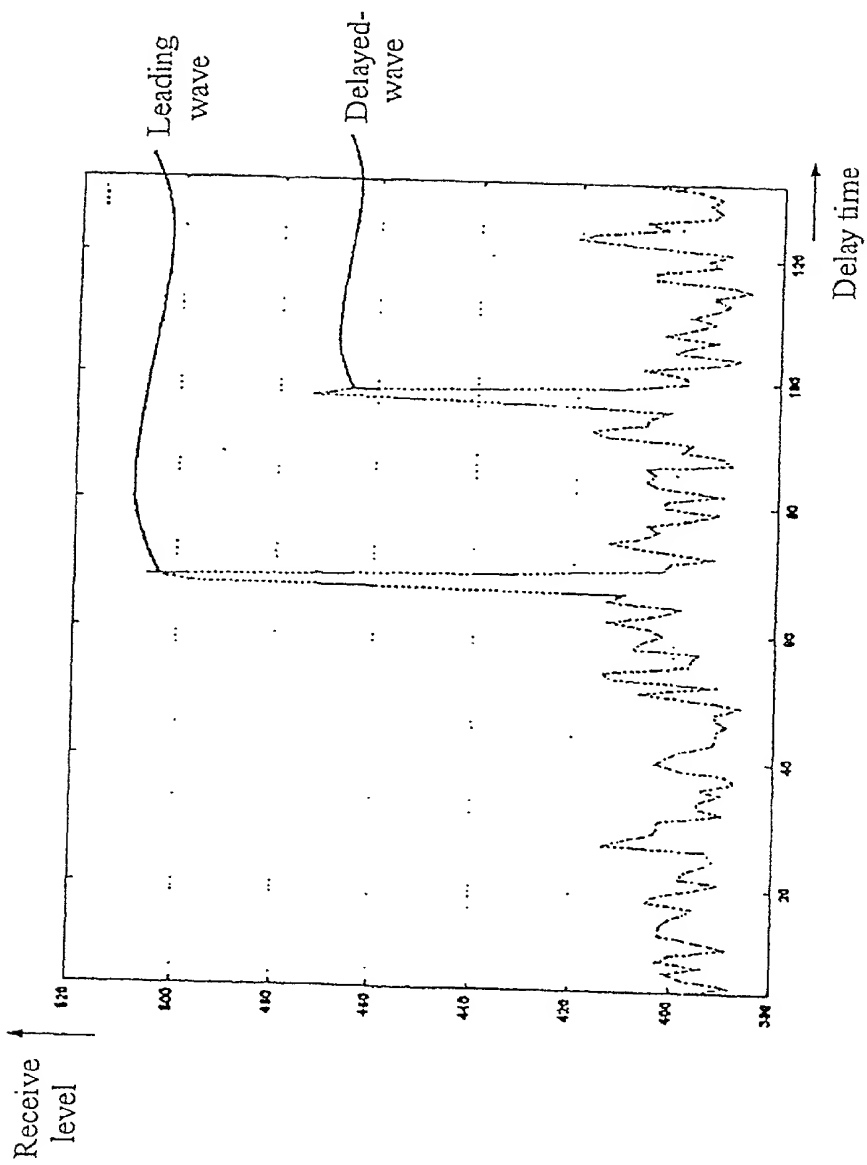


Fig. 9

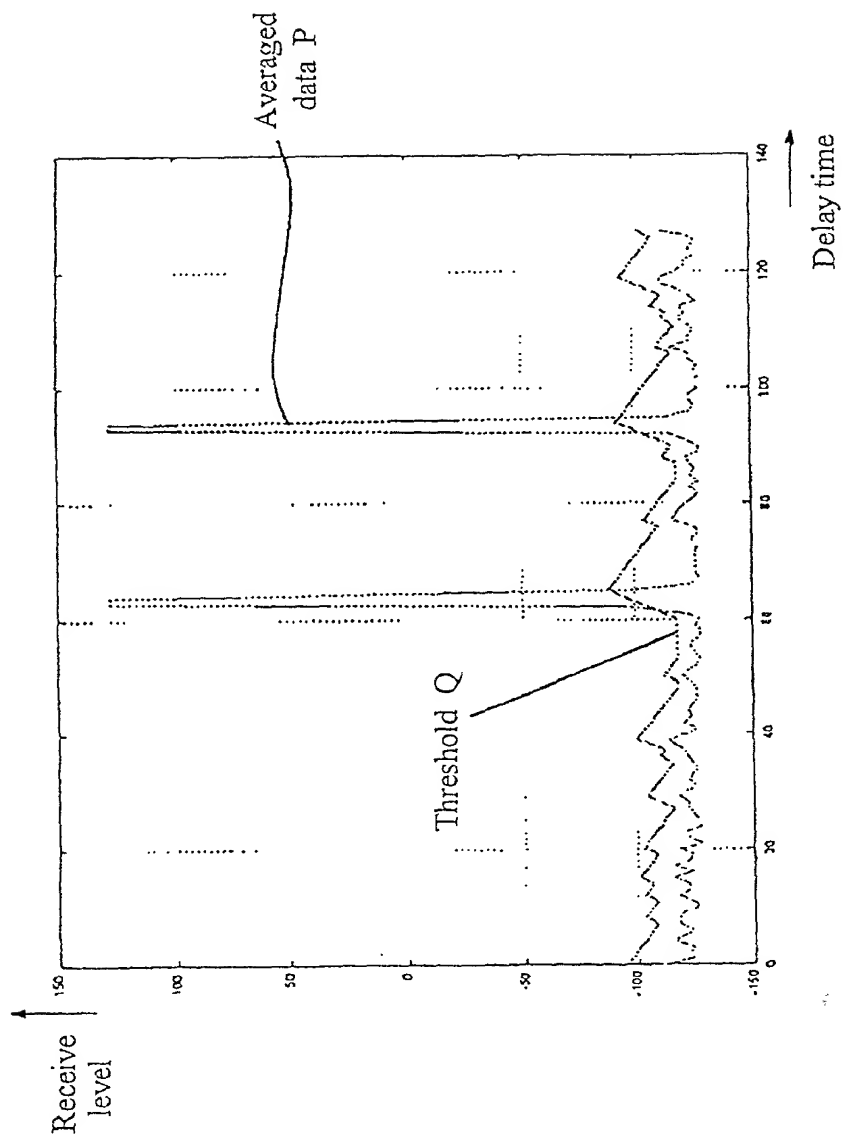


Fig. 10